Project

ADR GeoSTAR

Cross Correlator Test Report

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1 Introduction

1.1 Related Documentation

The tests performed and documented in this test report are based on the tests outline in the test procedure ADR_TPR_001A.

For reference to the correlator design, see ADR_MAN_001A.

1.2 Test Setup

A test PCB is used for managing clock signals, voltage levels and sampling. The test board has two input banks, each connected to 8 data and 4 clock inputs on the correlator ASIC. The voltage levels of the two banks can be individually tuned and offset compared to the correlator supply (VDDX). Remaining inputs can be set to either 1 or 0. There are two correlator clock paths on the board, one (LF) with a maximum frequency limited to around 2 GHz but where the delay of clocks to correlator and samplers can be programmed and another path (HF) where maximum frequency is considerably higher but where delays has to be handled externally. The HF clock path is connected through two SMA inputs on each input bank one for correlator clocking and one for sampler clocking. The LF path uses only one SMA input.

An Arduino Uno board with an ATmega328 microcontroller is used to control the correlator board and interface it to a PC through USB. It will receive simple commands such as correlate, readout etc. and handle signal assignments and timing.

A LabVIEW interface acts as a GUI and also handles functions for sweeps, readout reordering, some calculations and saving data to file.

Voltages are measured with an Agilent 34401A connected through GPIB to the LabVIEW interface. It can measure the voltage drop over a sense resistor connected to the supply of the correlator. This will make it possible to do current sweep measurements.

Power is supplied by a TTi CPX400. Two voltages are supplied; +4.5V and -5V both with a current limit set to 3A.

Correlator clock is supplied by an HP 83620 A synthesizer. The signal is split to four clock signals by a Pulsar PS4-26-452/10S splitter and fed to the four HF clock inputs. Additional tests has been performed with a Mini-Circuits ZFSC-8-43-S splitter to assure that the low frequency limit of the Pulsar splitter does not have an impact on the low frequency operation of the correlator.
Functionality Tests

1.2.1 Test F1

The correlator frequency is swept from 100MHz to 3500MHz in steps of 10MHz while the inputs to the correlator are held constant. The 16 SMA inputs are externally short-circuited to ground while all the other inputs are set to logic high.

For each frequency setting, a correlation measurement of 100ms is made.

The sweep measurement is repeated for seven different correlator core voltages (VDDX); 0.85V, 0.90V, 0.95V, 1.00V, 1.05V, 1.10V and 1.15V.

1.2.2 Test F2

The correlator frequency is set to constant 1000MHz. While all the inputs are identical to test F1, the correlation time (tCorr) is swept from 1ms to 1080ms in 1ms steps.

1.2.3 Test F3

The correlator frequency is swept from 100MHz to 3500MHz in steps of 10MHz while the inputs to the correlator are held constant. The 16 SMA inputs are connected to two different noise sources while the other inputs are set to logic high.

For each frequency setting, a correlation measurement of 100ms is made.

1.2.4 Test F4

Long time correlation test. This test is done to verify long time stability and error rate of the circuit. A one hour long correlation at 2 GHz will be performed with fixed inputs. The counters will loop to zero more than 6700 times, if any errors are present they will be accumulated and should show up if larger than 64.

1.2.5 Test F5

The clock to each of two inputs banks with SMA inputs can be tuned with a programmable delay circuit. If the phase relationship between different input banks to the correlator is too big, the correlation products will contain errors.

The correlator clock is set to 1GHz and the 16 SMA inputs are externally short-circuited to ground while all the other inputs are set to logic high. Correlations of 100µs are performed while one of the delay circuits, i.e. the clock to one input bank, is swept in steps of 11ps (the minimum step of the circuit).

1.2.6 Test F6

Input offset test. The correlator core voltage, VDDX, will be set to 1.0V and one of the input bank offsets will be centered to 0.5V. The swing of the input bank signals are 400mV p-p. The other input bank offset will be varied between -0.2 V and 0.2 V.

1.3 Expected Results

1.3.1 Test F1

It is expected that the correlator will function from some low frequency up to a few gigahertz. Simulations on the design suggested a top frequency as high as 4 GHz. It is also expected that at high frequencies the correlator will start to break down furthest away from the inputs due to skew while at low frequencies the errors could appear anywhere due to oscillation in the prescalers.

It is also assumed that the value of the correlation products will increase linearly as the correlation frequency is increased linearly and the correlation time is constant.

1.3.2 Test F2

The correlation time sweep should give a correlation product which linearly scales with correlation time and that is close to frequency times correlation time.

The maximum value of the correlation counters are 2^{30}. With a correlation frequency of 1000MHz, the counters will overflow for correlation time larger than 1074ms.

1.3.3 Test F3

For inputs with the same noise source, full correlation is expected, i.e. value zero in the counters. Due to the system being non-ideal, the realistic value should be between 90% and 97%.

For input pairs with different noise sources, 50% correlation is expected. Note that 0% correlation corresponds to two signals being true opposites, which implies that they are highly correlated.

1.3.4 Test F4

The test is performed at nominal core voltage level and at a frequency well below a known maximum, thus, no errors is expected.

1.3.5 Test F5

Simulation suggests that the correlator should function for skews up to 2 radians.

1.3.6 Test F6

The correlator should start to fail entirely where the offset goes below -0.2 V or above 0.2 V. It should also be more sensitive to higher frequencies the further away from centered it is because of changed duty cycle.

1.4 Results

1.4.1 Test F1

All cross correlation products with different inputs will contain high values while all correlation products of inputs with the same value will contain zero. Figure 1 shows one of the correlation products with different input values. As the correlator frequency increases, the value of the products does as well.

In Figure 2 the deviation of the actual measured product from the ideal (time times frequency) can be seen, the deviation is less than 0.16 % over the entire frequency range. It is also a systematic error in that it never drops below 0.145 %.

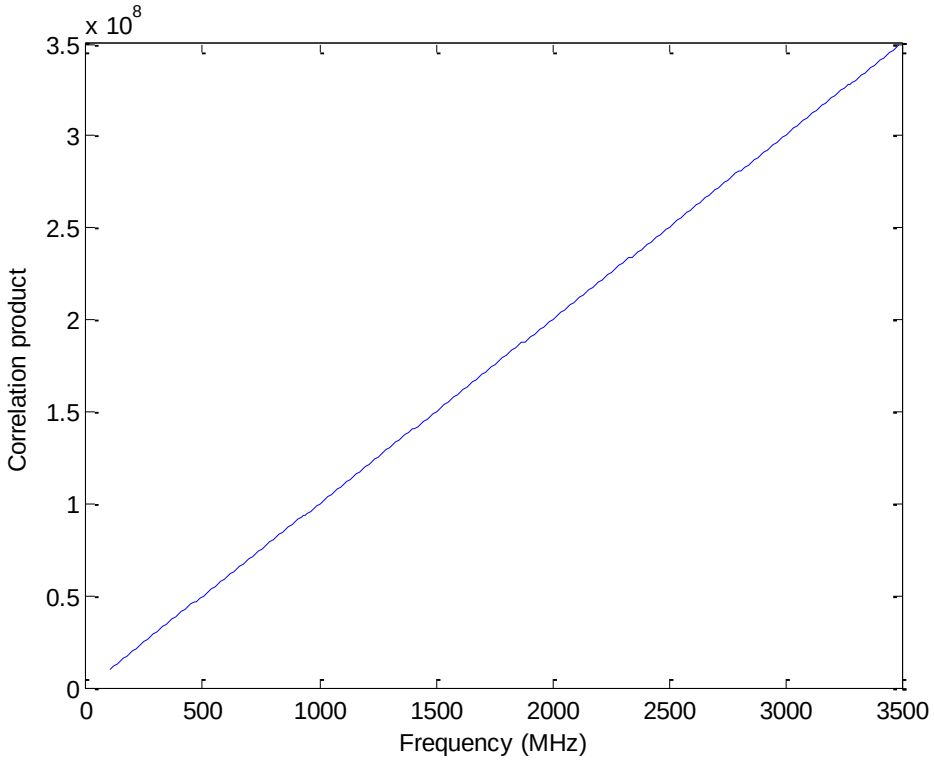

Figure 1 Anti correlation product of frequency sweep

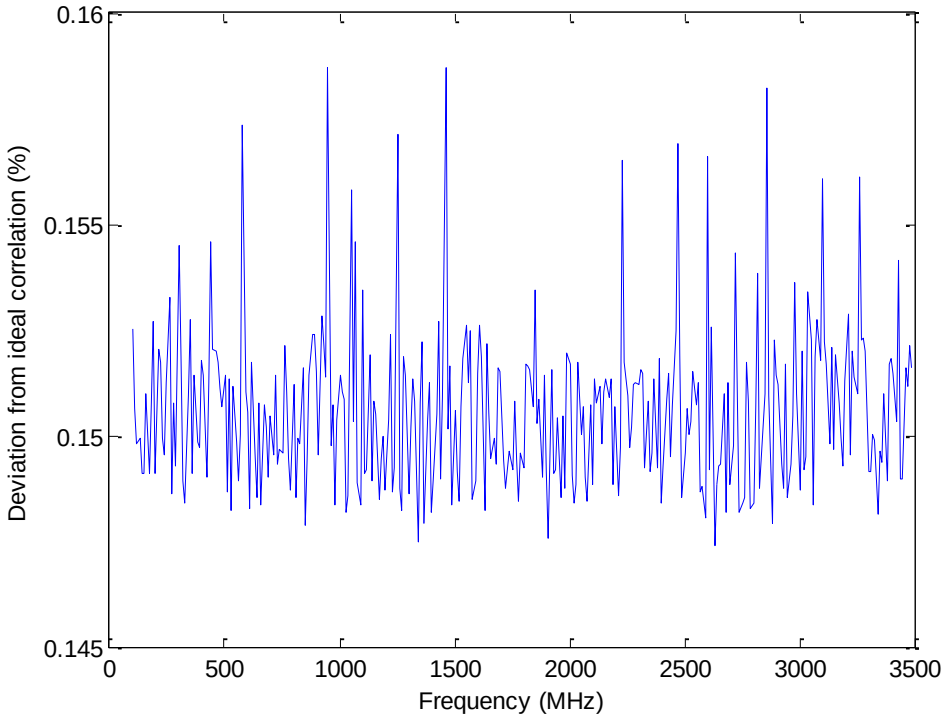

Figure 2 Deviation from ideal due to test setup

The number of errors in the correlator can be measured during this test by observing the correlation products which should be equal to zero and the correlation products that should be

equal to the correlation product seen in Figure 1. When they start to deviate from expected value we can assume that the functionality of the correlator is impaired. Figure 3 shows the sum of all correlation products which deviate from expected value. It can be seen that there are small amounts of errors for frequencies below 300MHz and above 2200GHz while none can be observed in between. It can also be seen that the correlator seems to work over the tested voltage range but the maximum frequency is lower with lower supply voltage.

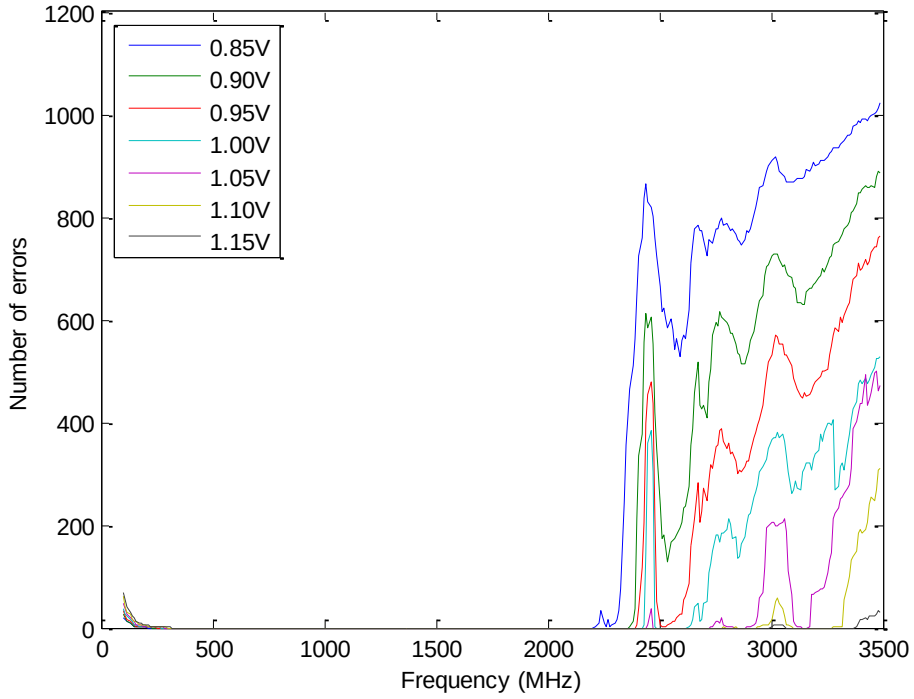

Figure 3 Error rate

1.4.2 Test F2

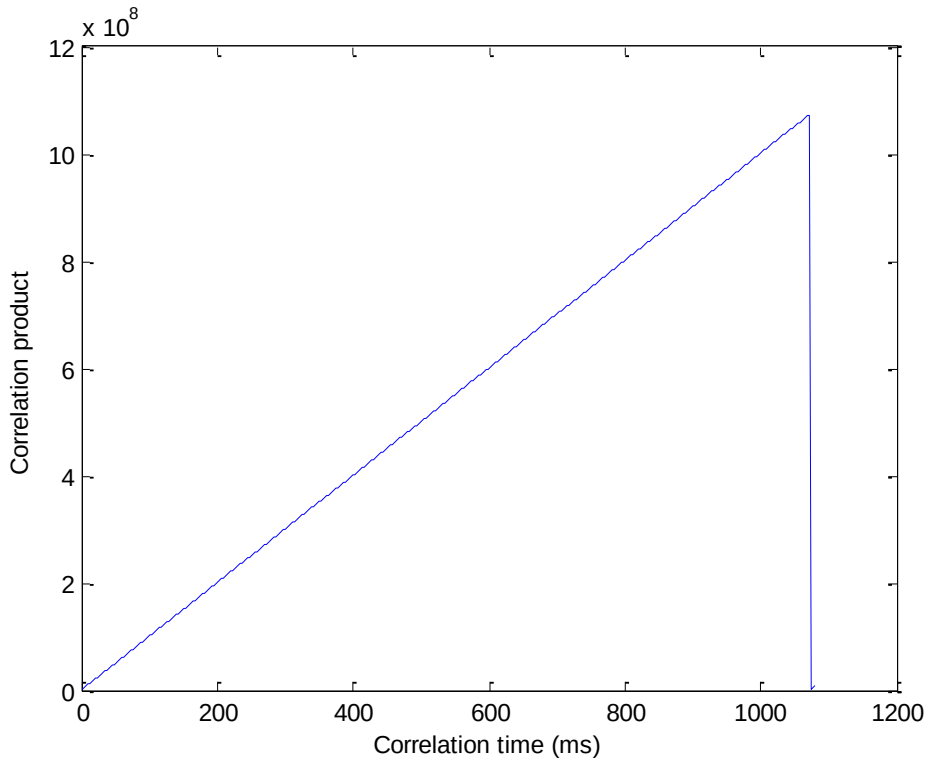

Figure 4 Anti correlation product from time sweep. The value of the correlation products increases linearly with the correlation time until the counters overflow after about 1074ms.

1.4.3 Test F3

Figure 5 shows the correlation between all signal pairs corresponding to the 16 inputs. In the orange scale are the pairs that have the same noise sources and should be correlated. In the blue scale are the pairs that have different noise sources. Brighter colour means higher frequency.

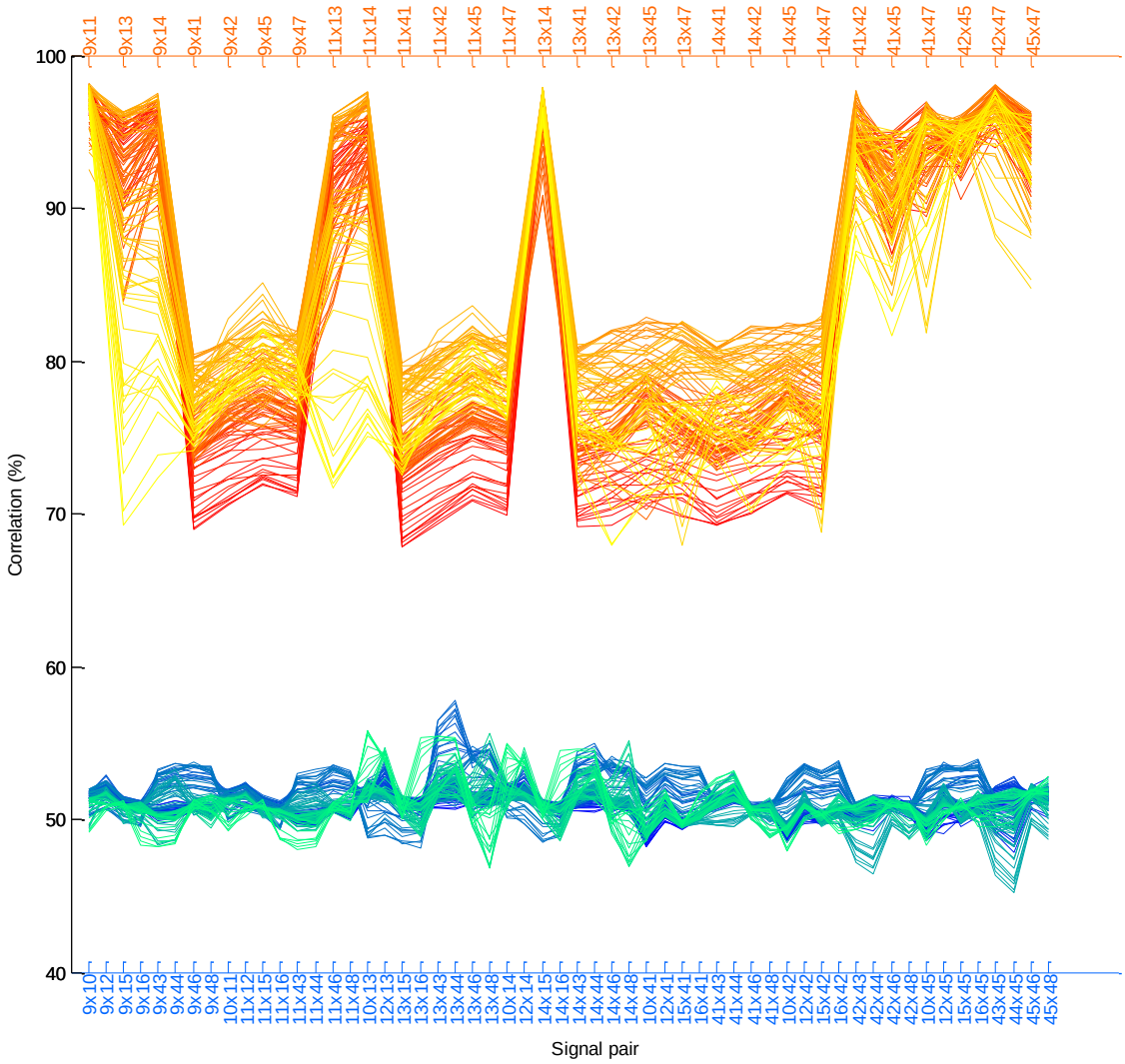

Figure 5 Correlation between signal pairs

1.4.4 Test F4

No errors were detected from the readout.

1.4.5 Test F5

Figure 6 shows the number of errors in the correlator as a function of the phase relationship between the two input banks with SMA inputs. It can be seen that there is a “clean” zone, centred around π/4. The zone is only slightly larger than 3π which is less than the expected 4π but not significantly.

The π/4 offset is probably due to offsets in components and PCB trace lengths.

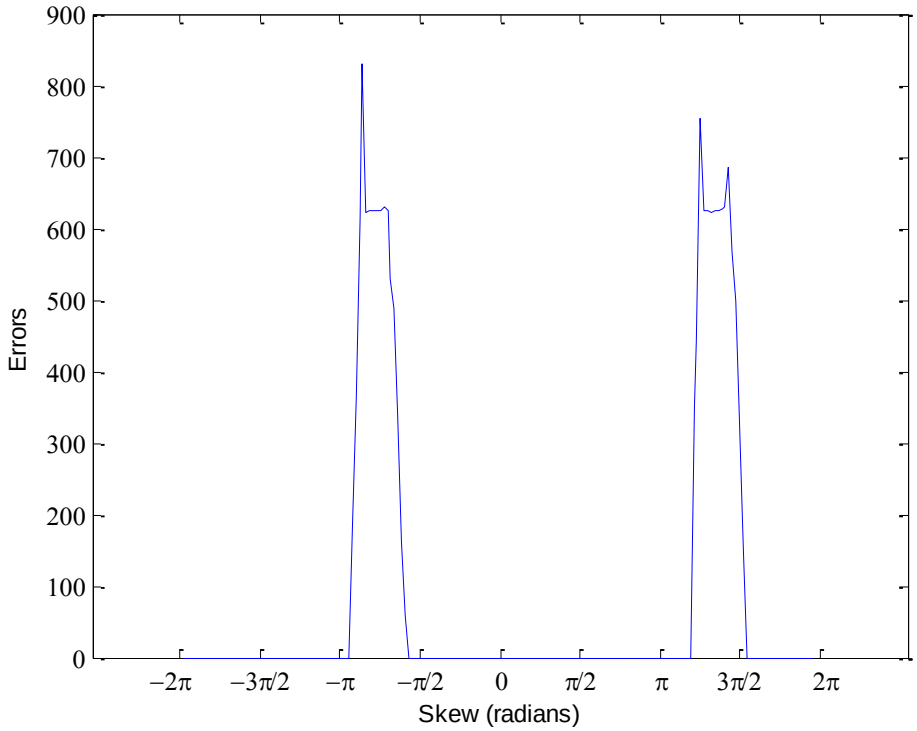

Figure 6 Correlator clock skew sweep

1.4.6 Test F6

Figure 7 and Figure 8 shows the low and high end of the input offset test. As can be seen offsetting the 400 mV_{p-p} input signal below VVDX/2-0.15 V or above VVDX/2+0.1 V causes problems for the correlator. A finer grained test around zero offset is shown in Figure 9; it seems a small negative offset has a positive effect on maximum frequency. Note that the offset is measured at the supply voltage of the input banks and not at the actual inputs of the correlator, i.e. the offset may be caused by differences on the PCB.

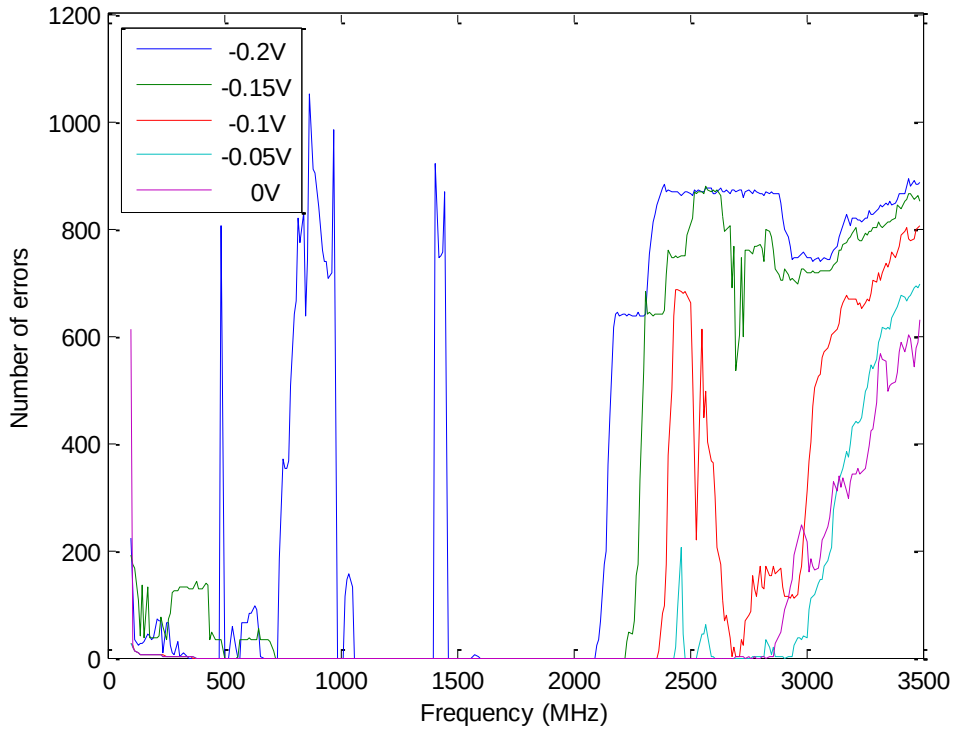

Figure 7 Input offset test low end

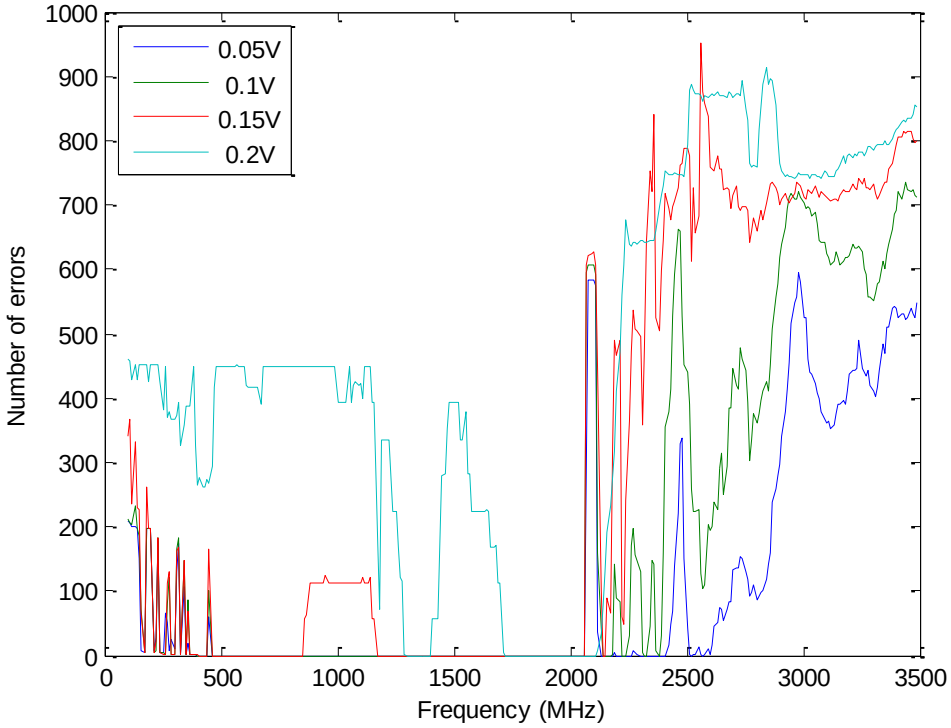

Figure 8 Input offset test high end

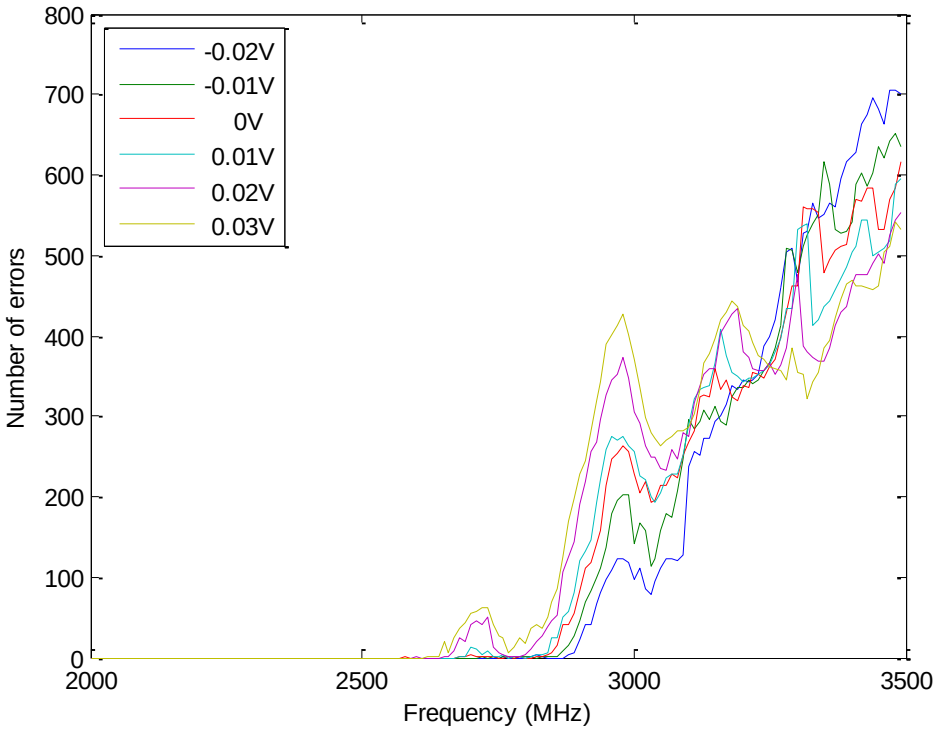

Figure 9 Fine grained input offset test

1.5 Conclusions

The correlator performs mostly as expected. The correlation products in test F1 and test F2 are calculated correctly. The maximum frequency is somewhat lower than simulated, but not necessarily lower than expected. There is some extra sensitivity around 2.4 GHz which shows up in test F1 but not for the same configuration (offset=0) in TEST 6. The skew tolerance in test F5 is close to expected. The zero skew point is not at the centre, this could be the result of test setup inaccuracies. No errors were detected in test F4 though there might still be errors assuming they are infrequent enough to not show up in the readout.

2 Power Consumption Test

2.1.1 Test P1

The correlator frequency is swept from 100MHz to 3500MHz in steps of 10MHz while the inputs to the correlator are held constant. The 16 SMA inputs are externally short-circuited to ground while all the other inputs are set to logic high.

The correlation time (tCorr) is about one second, in order to get a stable reading of the voltage drop across the sense resistor and therefore accurate current consumption estimation.

The sweep measurement is repeated for seven different correlator core voltages (VDDX); 0.85V, 0.90V, 0.95V, 1.00V, 1.05V, 1.10V and 1.15V.

2.1.2 Test P2

This test is similar to Test P1 but the 16 SMA connectors, which were previously connected to ground is now connected to two noise sources (8 inputs per noise source). This will cause the correlation paths to switch, as opposed to being constant.

The correlation time (tCorr) is about one second, in order to get a stable reading of the voltage drop across the sense resistor and therefore accurate current consumption estimation.

The sweep measurement is repeated for seven different correlator core voltages (VDDX); 0.85V, 0.90V, 0.95V, 1.00V, 1.05V, 1.10V and 1.15V.

2.1.3 Test P3

Power consumption measurements with noise, 0 and 1as inputs, all at 2 GHz clock frequency. The power consumption for the entire chip with uncorrelated noise is then calculated. Also, idle power measurement with no correlation but 2 GHz clock.

2.2 Expected Results

2.2.1 Test P1

The power should increase linearly with frequency and with the square of the voltage for as long as the correlator functionality is held.

2.2.2 Test P2

Same as in test P1 but with slightly higher values.

2.2.3 Test P3

Simulated power has been calculated to 0.13 mW/ch/GHz.

2.3 Results

2.3.1 Test P1

Figure 10 shows that the power consumption increases linearly with increasing frequency.

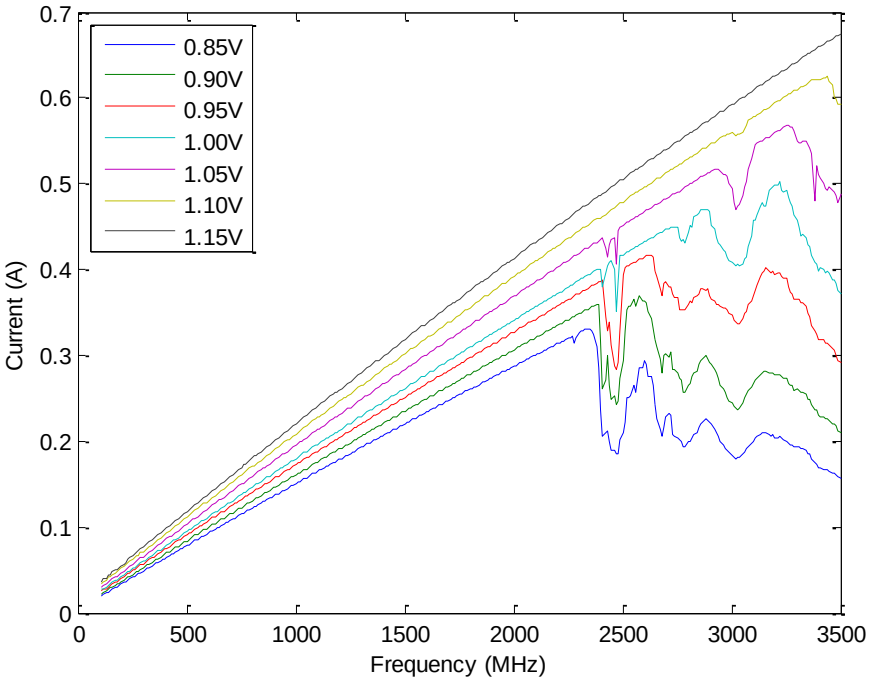

Figure 10 Supply current with fixed analog inputs

Figure 11 Power scaling with increased supply voltage at 2 GHzshows how the power scales with increased voltage at 2 GHz; the expected result was that the power would increase with the square of the voltage. This relationship is not obvious from the measured values since it does not span a wide range of voltages; an ideal square curve is plotted for reference. There are also a number of things that can cause mismatch between the curves such as the measurement accuracy and the chip not being entirely CMOS logic.

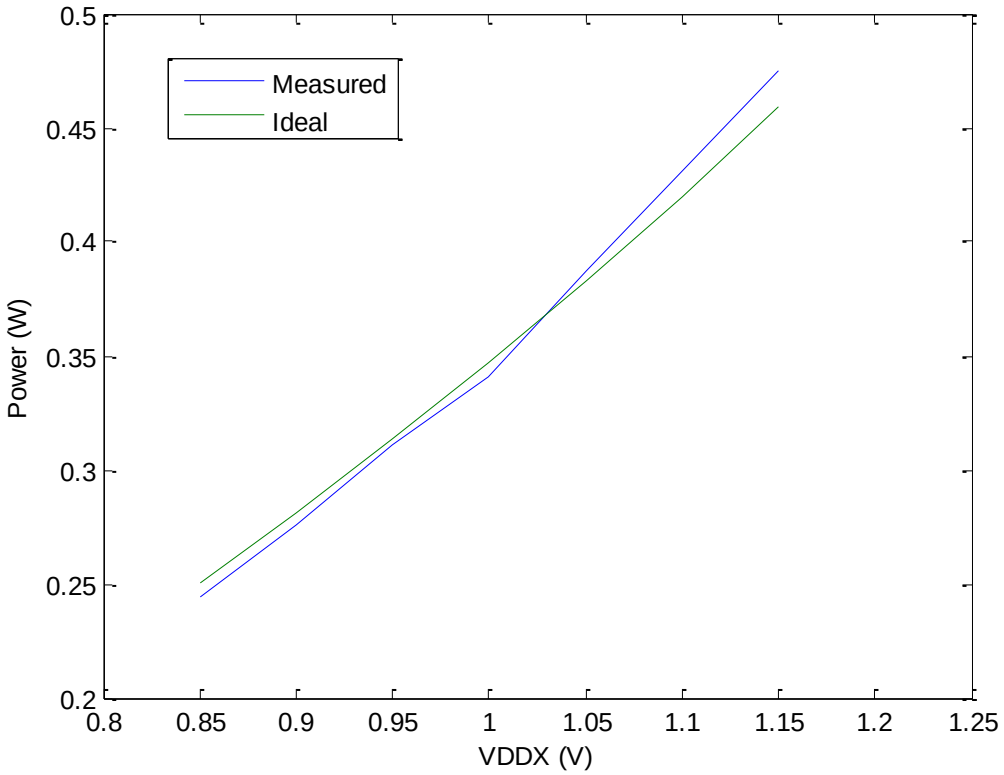

Figure 11 Power scaling with increased supply voltage at 2 GHz

2.3.2 Test P2

Figure 12 shows that the power consumptions increase linearly with increasing frequency.

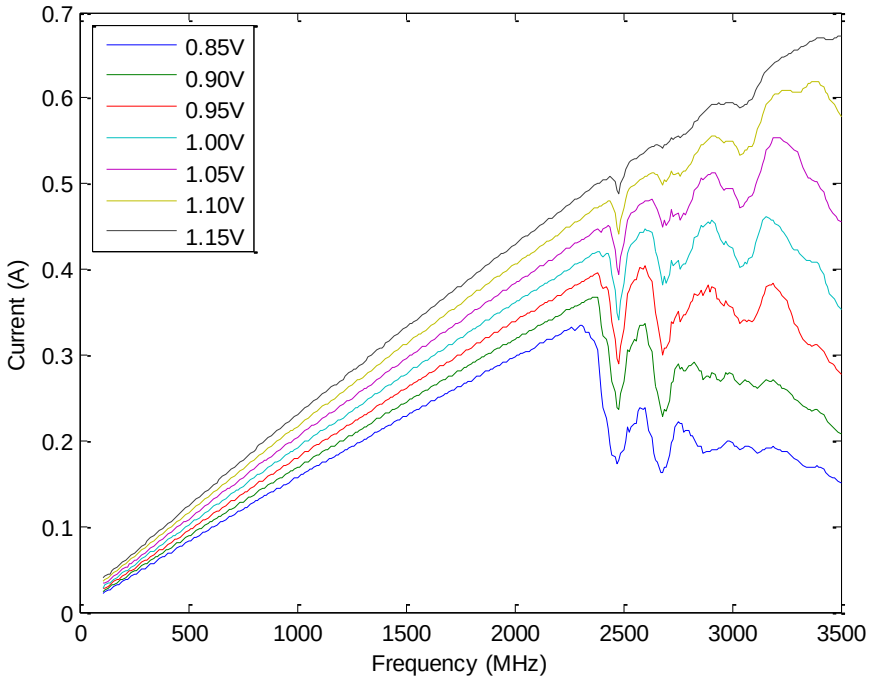

Figure 12 Supply current with noise on analog inputs

Figure 13 shows the difference between the measurement with and without noise on the 16 analog inputs. As can be seen the impact of adding noise is not profound.

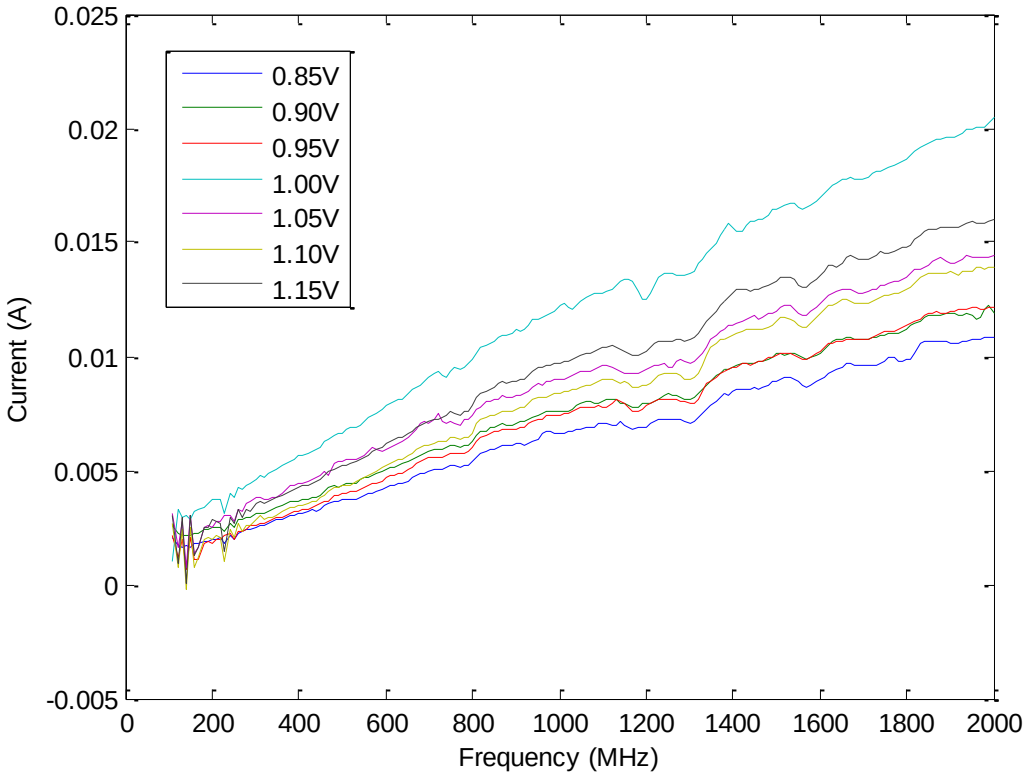

Figure 13 Difference between currents, with and without noise input

2.3.3 Test P3

The power consumption of the chip at 2 GHz with random noise on all 64 inputs is 0.53 W. This means 0.13mW/ch/GHz, where there are 2016 output channels on the chip.

When idle the chip consumes 0.04 W which corresponds to 9.0µW/ch/GHz.

2.4 Conclusions

In test P1 the current scales almost linearly with frequency for as long as the correlator is fully functional. The slight curvature that can be seen is most likely due to VDDX levels going down with increased current because of sense resistor voltage drop. The measured and calculated power consumption in test P3 is the same as what was predicted from simulations. The very low idle power is due to large parts of the chip using low leakage transistors.

3 Readout Test

The LabVIEW interface allows for comparing consecutive readout results, thereby testing the functionality of the readout logic. If two consecutive readouts without correlation between them are different, the readout has failed. Note that it is not guaranteed, although likely, that readout is successful if both are equal; as both can possibly fail in exactly the same way.

A divider, d, controls the SPI clock frequency; it can be set to 2^n. The SPI clock will then be 16/d MHz.

Doubleread is performed on different SPI clock frequencies and repeated with a number of correlator supply voltage levels. A check that the readout looks correct is also performed to minimize the risk of two identical erroneous readouts.

3.1 Expected Results

According to simulations and calculations the readout speed should be somewhere around 0.5 MHz at nominal voltage due to the way readout is performed internally. Transition times on the IO pads should be significantly faster than normally required for a 0.5 MHz clock.

3.2 Results

VDDX	Maximum SPI clock frequency (MHz)
0.80	No readout
0.85	0.25
0.90	0.25
0.95	0.25
1.00	0.5
1.05	0.5
1.10	0.5
1.15	0.5

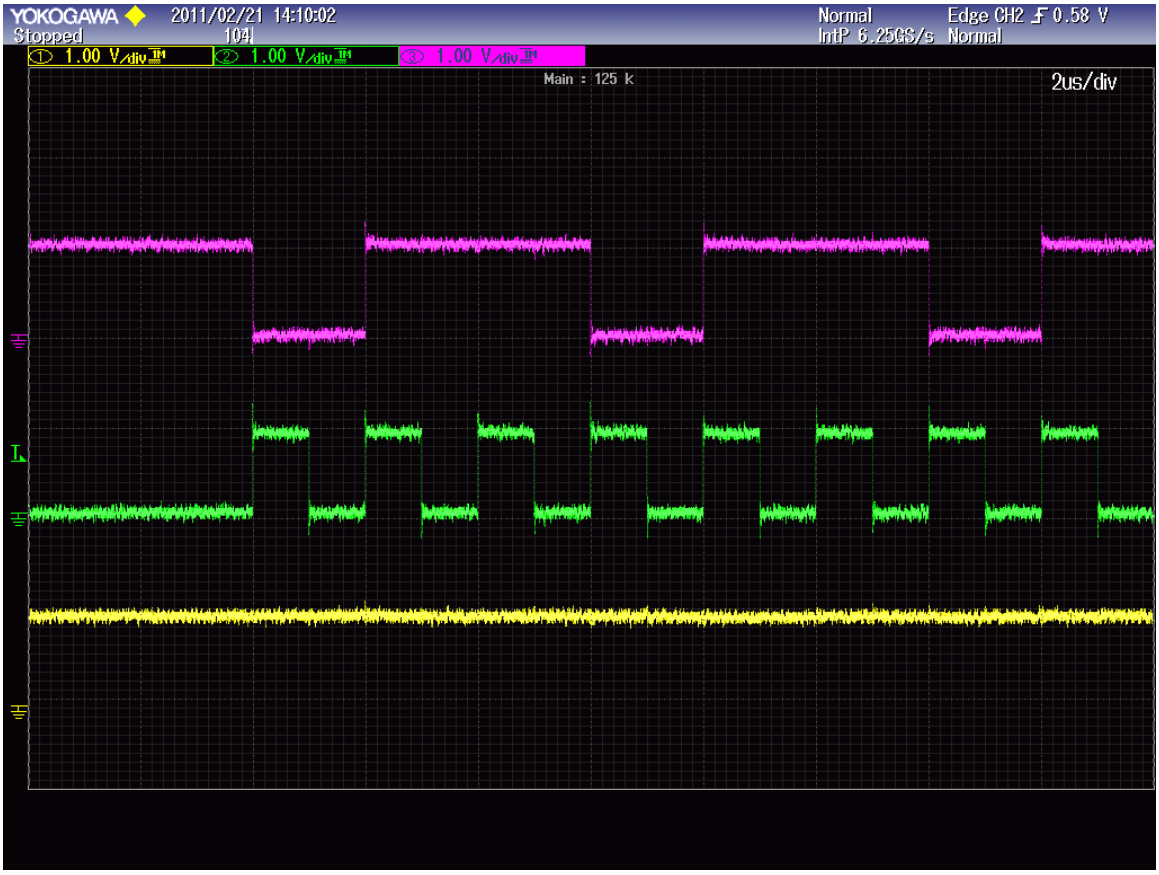

Figure 14 SPI readout probed with oscilloscope

3.3 Conclusions

Readout performance is not good but not unexpected either. Rise and fall times looks good as expected.

4 S-parameter Measurements

4.1 Results

Figure 15 shows the S11 parameters measured on the HF clock inputs. The measurement shows some bad results, especially for the input bank 1correlator clock.

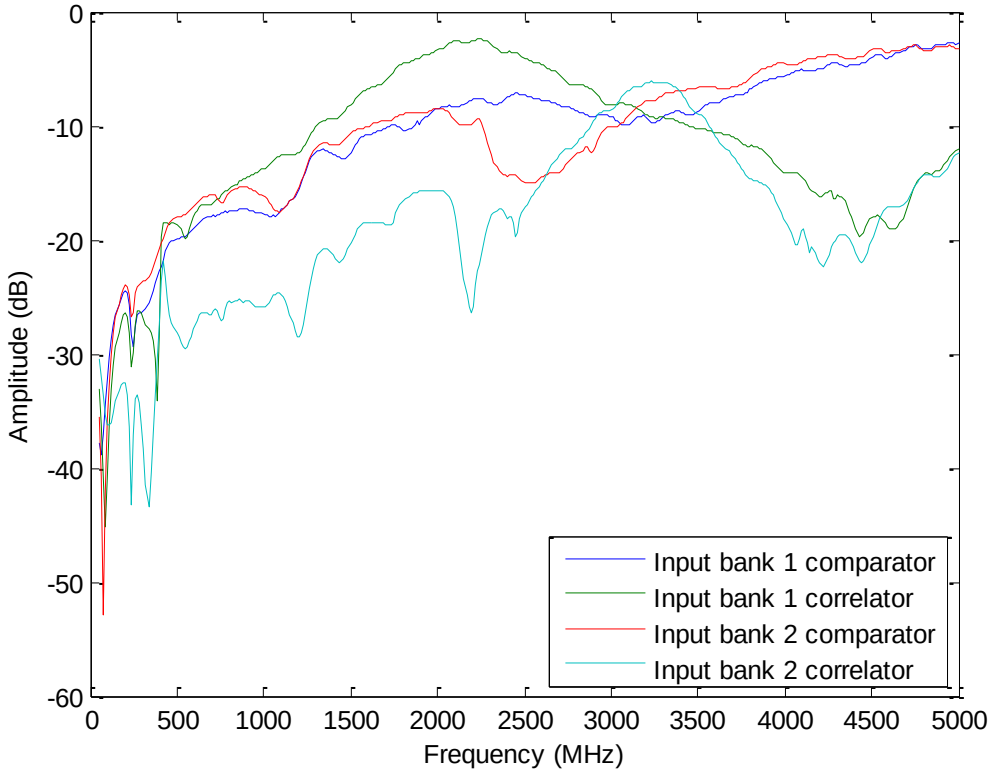

Figure 15 HF clock input S11 parameters

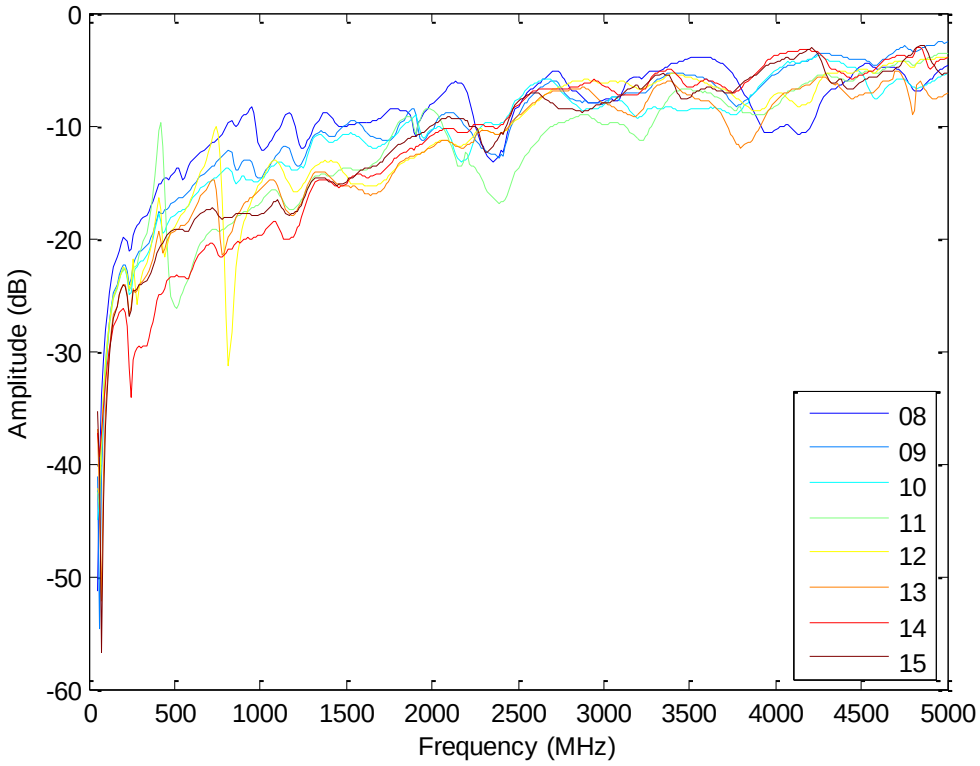

Figure 16 Input bank 1 S11 parameters

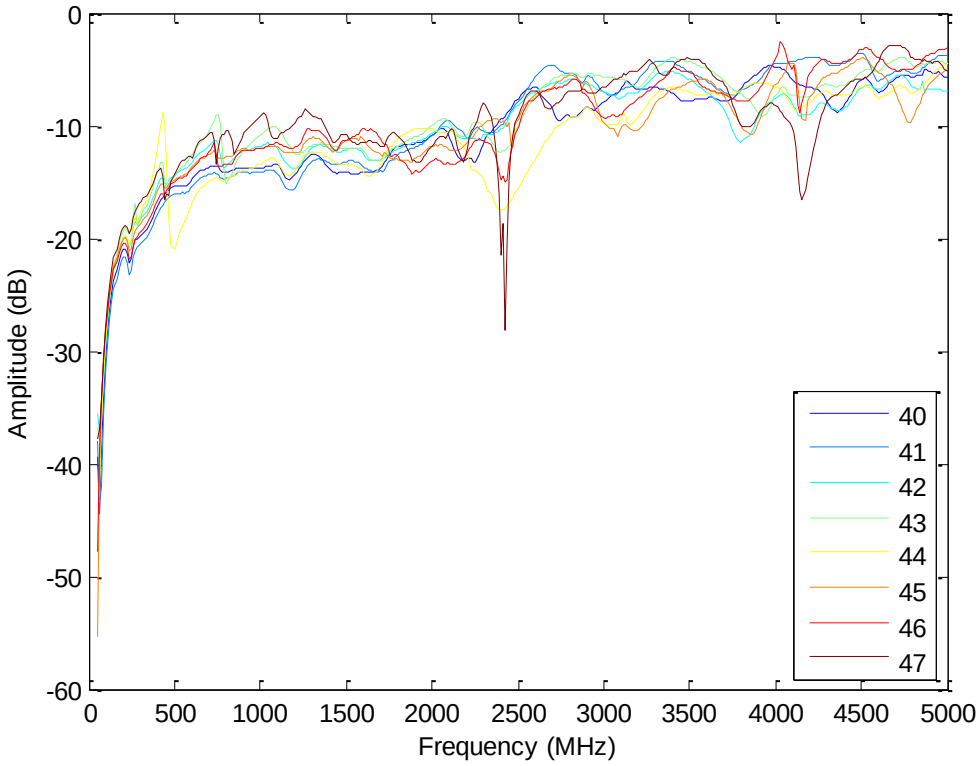

Figure 17 Input bank 2 S11 parameters

5 Lessons learned

There are a number of things that could be improved on the test setup. Measurements with a network analyzer pointed to some problems on the SMA input ports on the PCB both for signal inputs and clock inputs. The clock input might explain why there are problems around 2.4 GHz.

Another problem could be the reduced input swing to the correlator. The nominal IO voltage for the chip is $1.0V_{p\text{-}p}$ while the test board only drives it with 400 mV. Also the input signals from the comparators are only latched, meaning for half a cycle it will pass through whatever is on the inputs. This means that for noise inputs the correlator will only have half a clock cycle for decision time. The noise signals passing through to the correlator could also cause problems on the chip itself, high frequency switching of the input buffers means increased power consumption and could cause errors.